

## VERTICAL DEVICE 4F<sup>2</sup> EEPROM MEMORY

### Related Application

**[0001]** This application is related to U.S. Application Serial No. (Attorney Docket No. 400.264US01) filed \_\_\_\_\_, 200\_, entitled “4F<sup>2</sup> EEPROM NROM MEMORY ARRAYS WITH VERTICAL DEVICES,” which is commonly assigned.

### Technical Field of the Invention

**[0002]** The present invention relates generally to integrated circuits and in particular the present invention relates to EEPROM memory devices.

### Background of the Invention

**[0003]** Memory devices are typically provided as internal storage areas in the computer. The term memory identifies data storage that comes in the form of integrated circuit chips. There are several different types of memory used in modern electronics, one common type is RAM (random-access memory). RAM is characteristically found in use as main memory in a computer environment. RAM refers to read and write memory; that is, you can both write data into RAM and read data from RAM. This is in contrast to read-only memory (ROM), which permits you only to read data. Most RAM is volatile, which means that it requires a steady flow of electricity to maintain its contents. As soon as the power is turned off, whatever data was in RAM is lost.

**[0004]** Computers almost always contain a small amount of ROM that holds instructions for starting up the computer. Unlike RAM, ROM cannot be written to. An EEPROM (electrically erasable programmable read-only memory) is a special type non-volatile ROM that can be erased by exposing it to an electrical charge. EEPROM comprise a memory array which includes a large number of memory cells having electrically isolated gates (floating gates). Data is stored in the memory cells in the form of charge on the floating gates. Each of the cells within an EEPROM memory array can be electrically programmed in a random basis by charging the floating gate. The charge can also be randomly removed from the floating gate by an erase operation.

Charge is transported to or removed from the individual floating gates by specialized programming and erase operations, respectively.

**[0005]** Yet another type of non-volatile memory is a Flash memory. A Flash memory is a type of EEPROM that is typically erased and reprogrammed in blocks instead of one byte at a time. A typical Flash memory comprises a memory array, which includes a large number of memory cells. Each of the memory cells includes a floating gate field-effect transistor capable of holding a charge. The data in a cell is determined by the presence or absence of the charge in the floating gate. The cells are usually grouped into sections called “erase blocks.” Each of the cells within an erase block can be electrically programmed in a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation, wherein all floating gate memory cells in the erase block are erased in a single operation.

**[0006]** The memory cells of both an EEPROM memory array and a Flash memory array are typically arranged into either a “NOR” architecture (each cell directly coupled to a bit line) or a “NAND” architecture (cells coupled into “strings” of cells, such that each cell is coupled indirectly to a bit line and requires activating the other cells of the string for access).

**[0007]** A problem in floating gate memory cell arrays is the issue of overerased memory cells. A floating gate memory cell is structurally similar to a MOSFET transistor, with a control gate separated from a channel, source, and drain by an insulator. In addition, embedded in the insulator is an isolated floating gate. As in a MOSFET transistor, current flows when the floating gate memory cell/transistor is selected or activated, charge trapped on the floating gate affects the amount of current flow in the floating gate transistor, effectively raising or lowering its threshold. In programming or erasing a floating gate memory cell, charge is transported to or from the electrically insulated floating gate of the floating gate transistor. If too much charge is removed from the floating gate of the floating gate transistor/memory cell it will flow current even when it is not selected. Floating gate transistors in this overerased state can affect current flow on shared bitlines and/or memory strings and thus potentially

corrupt data read from other memory cells these common bitlines and/or memory strings.

**[0008]** In addition, as integrated circuit processing techniques improve, manufacturers try to reduce the feature sizes of the devices produced and thus increase the density of the IC circuits and memory arrays. In floating gate memory arrays in particular, the channel length of the floating gate memory cells that make up the memory array and spacing between memory cells in the strings have a large effect on the number of memory cells that can be placed in a given area and thus a direct impact on the density of the array and size of the resulting memory device.

**[0009]** For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a method and architecture for producing a more closely spaced and, thus, higher density floating gate memory array with improved overerasure handling properties.

#### Summary of the Invention

**[0010]** The above-mentioned problems with producing a more closely spaced and higher density floating gate memory array with improved overerasure handling properties and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

**[0011]** EEPROM memory devices and arrays, in accordance with embodiments of the present invention, facilitate the utilization of vertical floating gate memory cells and select gates in NOR or NAND high density memory architectures. Memory embodiments of the present invention utilize vertical select gates and floating gate memory cells to form NOR and NAND architecture memory cell strings, segments, and arrays. These memory cell architectures allow for improved high density memory devices or arrays with integral select gates that can take advantage of the feature sizes semiconductor fabrication processes are generally capable of and allow for appropriate device sizing for operational considerations. The memory cell architectures also allow for mitigation of disturb and overerasure issues by placing the floating gate memory

cells behind select gates that isolate the memory cells from their associated bit lines and/or source lines.

**[0012]** For one embodiment, the invention provides a memory device comprising a NOR architecture floating gate memory array formed on a substrate having a plurality of pillars and associated intervening trenches, and a plurality of memory cell structures. Each memory cell structure having a floating gate memory cell, wherein the floating gate memory cell is formed vertically on a first sidewall of a trench, and a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the floating gate memory cell by a source and drain region formed at the bottom of the trench.

**[0013]** For another embodiment, the invention provides a floating gate memory cell structure comprising a substrate, having two raised areas, defining a trench therebetween. A floating gate memory cell is formed vertically on a first sidewall of the trench, and a select gate memory cell is formed vertically on a second sidewall of the trench. Where the floating gate memory cell is coupled to the select gate by source and drain region formed at the bottom of the trench.

**[0014]** For yet another embodiment, the invention provides a method of forming a floating gate memory cell structure comprising forming two raised areas on a substrate, the raised areas defining an associated intervening trench. Forming a floating gate memory cell on a first sidewall of the trench and a select gate on a second sidewall of the trench, and forming a source and drain region at the bottom of the associated intervening trench.

**[0015]** For a further embodiment, the invention provides a NAND architecture floating gate memory cell string comprising a substrate, having two or more raised areas, defining trenches therebetween. A plurality of floating gate memory cells are formed vertically on the sidewalls of the trenches, wherein the plurality of floating gate memory cells are coupled in a serial string by source/drain regions formed at the top of the two or more raised areas and at the bottom of the one or more trenches. A first floating gate memory cell is coupled to a first select gate, where the first select gate is formed vertically on a sidewall of a selected trench.

**[0016]** For yet a further embodiment, the invention provides a memory device comprising a NAND architecture memory array formed on a substrate having a plurality of pillars and associated intervening trenches. The memory array having a plurality of floating gate memory cells formed vertically on the sidewalls of the plurality of pillars and trenches, wherein the plurality of floating gate memory cells are coupled into a plurality of NAND architecture memory strings by source/drain regions formed at the top of the plurality of pillars and at the bottom of the associated trenches. A first floating gate memory cell of each string of the array is coupled to a first vertical select gate and a last floating gate memory cell of each NAND architecture memory string is coupled to a second vertical select gate. The memory device also comprises a control circuit, a row decoder, a plurality of word lines coupled to the row decoder, a plurality of select lines, at least one bitline, and at least one source line. Wherein each word line is coupled to one or more control gates of one or more floating gate memory cells, where each of the one or more floating gate memory cells is from a differing string of the plurality of NAND architecture memory strings. Each select line is coupled to one or more select gates. The at least one bitline is coupled to a drain of the first select gate of each string of the plurality of NAND architecture memory strings. And the at least one source line is coupled to a source of the second select gate of each string of the plurality of NAND architecture memory strings.

**[0017]** For another embodiment, the invention provides a method of forming a NAND architecture memory cell string comprising forming one or more raised areas on a substrate, the raised areas defining associated intervening trenches, forming a plurality of floating gate memory cells on the sidewalls of the one or more raised areas, forming one or more source/drain regions on the top of the one or more raised areas and at the bottom of the one or more associated intervening trenches, and forming a first vertical select gate coupled to a first floating gate memory cell of the NAND architecture memory string and a second vertical select gate coupled to a last floating gate memory cell of the NAND architecture memory string.

**[0018]** Other embodiments are also described and claimed.

### Brief Description of the Drawings

[0019] Figures 1A and 1B detail erase operations in floating gate memory cells.

[0020] Figures 2A-2C detail a planar NAND floating gate memory array of the prior art.

[0021] Figures 3A-3C detail a planar NOR floating gate memory array of the prior art.

[0022] Figures 4A-4C detail vertical NOR floating gate memory array and cells in accordance with embodiments of the present invention.

[0023] Figures 5A and 5B detail vertical NAND floating gate memory array and cells in accordance with embodiments of the present invention.

[0024] Figures 6A-6C detail formation of a vertical NAND architecture floating gate memory array having floating gates and select gates in accordance with embodiments of the present invention.

[0025] Figure 7 details a block diagram of an electronic system in accordance with embodiments of the present invention.

### Detailed Description of the Invention

[0026] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The terms wafer and substrate used previously and in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor, as well as other semiconductor structures well known to one

skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the claims and equivalents thereof.

**[0027]** EEPROM memory devices and arrays, in accordance with embodiments of the present invention, facilitate the utilization of vertical floating gate memory cells and select gates in NOR or NAND high density memory architectures. Memory embodiments of the present invention utilize vertical select gates and floating gate memory cells to form NOR and NAND architecture memory cell segments and arrays. These memory cell architectures allow for improved high density memory devices or arrays with integral select gates that can take advantage of the feature sizes semiconductor fabrication processes are generally capable of and allow for appropriate device sizing for operational considerations. The memory cell architectures also allow for mitigation of disturb and overerasure issues by placing the floating gate memory cells behind select gates that isolate the memory cells from their associated bit lines and/or source lines.

**[0028]** As stated above, as integrated circuit processing techniques improve, manufacturers try to reduce the feature sizes of the devices produced and thus increase the density of the IC circuits and memory arrays. In many cases, the feature sizes of the devices are limited by the device characteristics before the minimum feature size that the process is capable of is reached. In both NAND and NOR architecture EEPROM memory arrays, as the channel length is reduced and the spacing between memory cells in the strings are reduced, a minimum size is reached that is primarily dictated by the operational characteristics of the floating gate memory cell devices that make up the memory array. As a result, the maximum density of an array of memory cells is limited even if the process technology can attain even smaller features and/or channel lengths. In particular, this is an issue in higher capacity memory types where small changes in the memory cell footprint (e.g., memory cell channel widths) and the cell density in the array can have a large effect on the overall array size and the resulting storage capacity.

**[0029]** As stated above, programming a floating gate memory cell involves the insertion and storage of charge on the memory cell's floating gate. Typically, a floating gate memory cell electrically operates as an enhancement type MOS transistor, requiring a positive voltage applied across the gate and channel to flow current. The presence, or lack thereof, of a trapped charge on the floating gate of the floating gate transistor/memory cell alters the threshold voltage characteristics of this transistor and thus the amount of current the transistor will flow at a given gate channel voltage. The effective threshold voltage of the floating gate transistor memory cell increases with storage of electrons on the floating gate and decreases with the removal of stored charge. Reading floating gate memory cells in EEPROM memory arrays is then accomplished by accessing a memory cell with selected read voltage levels on the control gate and source line. The stored data is then typically sensed from the amount of current the floating gate memory cell flows through the coupled bit line.

**[0030]** In programming floating gate memory cells in EEPROM memory arrays, electrons are typically transferred to the floating gate of the memory cell by one of Fowler-Nordheim tunneling (FN-Tunneling) or channel hot electron injection (HEI). Other forms of programming floating gate memory cells, such as, substrate enhanced hot electron injection (SEHE), are also known and utilized. FN-Tunneling is typically accomplished by applying a positive control gate voltage on the floating gate memory cell with respect to its substrate or surrounding P-well to tunnel inject electrons to the floating gate. Channel hot electron injection (HEI) is typically accomplished by applying a positive voltage on the control gate and drain of the floating gate memory cell and a low voltage or ground on the source to inject electrons to the floating gate. In many cases the programming voltages are iteratively pulsed and the memory cell read to check the programming process and more accurately program the floating gate memory cell.

**[0031]** Erasure of the floating gate memory cells of EEPROM memory arrays is typically accomplished by conventional tunneling or negative voltages applied to the control gate voltages with respect to the substrate or surrounding isolation P-well. Alternatively, other forms of erasure, such as, substrate enhanced band to band

tunneling induced hot hole injection (SEBBHH) can also be used for floating gate memory cell erasure. To ensure uniformity, in many cases the EEPROM memory programs all the floating gate memory cells in the data segment to be erased before applying the voltages to erase the memory cells. As with programming, the erasure voltages are typically iteratively pulsed and the memory cells checked after each pulse to verify erasure and return of the floating gate memory cells to an un-programmed threshold voltage state.

**[0032]** Unfortunately, it is possible, during an erasure process, for too much charge to be removed from the floating gate of a floating gate memory cell transistor placing it in to an “overerased” state. In such cases, enough charge is removed that the threshold voltage of the floating gate memory cell transistor is altered so that it operates as a depletion mode device, requiring a negative control gate-channel voltage to be applied to shut off current flow. In this state, the floating gate memory cell transistor will flow a current even when it has not been selected by the memory, unless a negative voltage is applied to the control gate with respect to the source. This “overerased” state and the resulting current flow when the overerased floating gate memory cell is unselected can interfere with attempts to read the values of other floating gate memory cells that share the common bit lines with it, corrupting the read data.

**[0033]** Complicating the issue of overerasure in floating gate memory cells is that not all floating gate memory cells erase (remove charge from their floating gates) at the same rate of speed. Typically, one or more “fast erasing” memory cells will erase more quickly than the others of the group of cells selected for erasure. To minimize the possibility of inadvertently overerasing this group of fast erasing floating gate memory cells most EEPROM and Flash memory devices/arrays typically utilize the complex and time consuming iterative erase voltage pulse-memory cell verify process noted above to erase its floating gate memory cells.

**[0034]** Figure 1A details a chart of a distribution of threshold voltages 100 of floating gate memory cells in a given array, showing distribution bell curves of the threshold voltages of floating gate memory cells placed in a programmed 102 and erased 104 state as might be typical of a floating gate memory device. Figure 1A also

details a number of erased cells that have been inadvertently placed in an overerased (depletion mode) 106 state. Figure 1B details a bit line 110 of a memory array 112 and the current flow 114 through an overerased floating gate memory cell 116 that has not been selected/activated for reading.

**[0035]** An additional issue that can affect the memory cells of an EEPROM or Flash memory array is “disturb.” Disturb typically happens when the elevated voltages used to program or erase a floating gate memory cell segment or erase block “disturb” the programmed values stored in other floating gate memory cells corrupting them and causing errors when they are later read. These inadvertently disturbed cells typically share common word lines, bit lines, or source lines with the memory cells that are being programmed or erased.

**[0036]** By constructing their floating gate memory cells vertically and isolating them with select gates, embodiments of the present invention allow for increases in memory array cell density and improved utilization of process minimum feature size capabilities, while maintaining the size of the memory cell channel to allow for appropriate device operation. In addition, by increasing the available surface area for transistors and incorporating select gates, which are also constructed in a vertical manner, embodiments of the present invention mitigate issues with overerasure and disturb, allowing for greater reliability and faster programming and erasure.

**[0037]** As previously stated, the two common types of EEPROM and Flash memory array architectures are the “NAND” and “NOR” architectures, so called for the similarity each basic memory cell configuration has to the corresponding logic gate design. In the NOR array architecture, the floating gate memory cells of the memory array are arranged in a matrix similar to RAM or ROM. The gates of each floating gate memory cell of the array matrix are coupled by rows to word select lines (word lines) and their drains are coupled to column bit lines. The source of each floating gate memory cell is typically coupled to a common source line. The NOR architecture floating gate memory array is accessed by a row decoder activating a row of floating gate memory cells by selecting the word line coupled to their gates. The row of selected memory cells then place their stored data values on the column bit lines by

flowing a differing current from the coupled source line to the coupled column bit lines depending on their programmed states. A column page of bit lines is selected and sensed, and individual data words are selected from the sensed data words from the column page and communicated from the memory.

**[0038]** An EEPROM or Flash NAND array architecture also arranges its array of floating gate memory cells in a matrix such that the gates of each floating gate memory cell of the array are coupled by rows to word lines. However each memory cell is not directly coupled to a source line and a column bit line. Instead, the memory cells of the array are arranged together in strings, typically of 8, 16, 32, or more each, where the memory cells in the string are coupled together in series, source to drain, between a common source line and a column bit line. This allows a NAND array architecture to have a higher memory cell density than a comparable NOR array, but with the cost of a generally slower access rate and programming complexity.

**[0039]** A NAND architecture floating gate memory array is accessed by a row decoder activating a row of floating gate memory cells by selecting the word select line coupled to their gates. In addition, the word lines coupled to the gates of the unselected memory cells of each string are also driven. However, the unselected memory cells of each string are typically driven by a higher gate voltage so as to operate them as pass transistors and allowing them to pass current in a manner that is unrestricted by their stored data values. Current then flows from the source line to the column bit line through each floating gate memory cell of the series coupled string, restricted only by the memory cells of each string that are selected to be read. This places the current encoded stored data values of the row of selected memory cells on the column bit lines. A column page of bit lines is selected and sensed, and then individual data words are selected from the sensed data words from the column page and communicated from the memory device.

**[0040]** Figures 2A, 2B, and 2C show a simplified planar NOR floating gate memory array of a EEPROM or Flash memory device of the prior art. Figure 2A details a top view of a planar NOR architecture floating gate memory array 200, a side view of the planar NAND floating gate memory array 200 is detailed in Figure 2B. In Figures 2A

and 2B, floating gate memory cells 202 are coupled together in a NOR architecture memory array having bit lines 212, source lines 214, and word lines 206. The bit lines 212 and source lines 214 are formed locally from N+ doped regions deposited in the substrate 208. Each floating gate memory cell 202 has a gate-insulator stack formed between the N+ doped regions of a bit line 212 and a source line 214, utilizing the N+ doped regions as a drain and source respectively. The gate-insulator stack is made of a tunnel insulator on top of a substrate 208, a floating gate formed on the tunnel insulator, an intergate/interpoly insulator formed over the floating gate, and a control gate 206 (typically formed integral to the word line 206, also known as a control gate line) formed over the intergate/interpoly insulator. Figure 2C details an equivalent circuit schematic 220 of the NOR architecture floating gate memory array 200, showing floating gate memory cells 202 coupled to the bit lines, source lines, word lines, and substrate connection 222.

**[0041]** Figures 3A, 3B, and 3C show a simplified planar NAND floating gate memory array of a EEPROM or Flash memory device of the prior art. Figure 3A details a top view of a planar NAND floating gate memory string 304 of a NAND architecture floating gate memory array 300, a side view of the planar NAND floating gate memory string 304 is detailed in Figure 3B. In Figures 3A and 3B, a series of floating gate memory cells 302 are coupled together in a series NAND string 304 (typically of 8, 16, 32, or more cells). Each floating gate memory cell 302 has a gate-insulator stack that is made of a tunnel insulator on top of a substrate 308, a floating gate formed on the tunnel insulator, an intergate/interpoly insulator formed over the floating gate, and a control gate 306 (typically formed in a control gate line, also known as a word line) formed over the intergate/interpoly insulator. N+ doped regions are formed between each gate insulator stack to form the source and drain regions of the adjacent floating gate memory cells, which additionally operate as connectors to couple the cells of the NAND string 304 together. Select gates 310, that are coupled to gate select lines, are formed at either end of the NAND floating gate string 304 and selectively couple opposite ends of the NAND floating gate string 304 to a bit line contact 312 and a source line contact 314. Figure 3C details an equivalent circuit

schematic 320 of the NAND architecture floating gate memory string 304, showing floating gate memory cells 302 and substrate connection 322.

**[0042]** Embodiments of the present invention utilize vertical floating gate memory cells and vertical gate structures. Methods of forming vertical memory cells are detailed in United States Patent No. 5,936,274, titled “High density flash memory”, issued August 10, 1999, which is commonly assigned. Methods of forming vertical split control gates are detailed United States Patent No. 6,150,687, titled “Memory cell having a vertical transistor with buried source/drain and dual gates”, issued November 21, 2000, and United States Patent No. 6,072,209, titled “Four F<sup>2</sup> folded bit line DRAM cell structure having buried bit and word lines”, issued June 6, 2000, which are also commonly assigned.

**[0043]** Figures 4A-4C detail vertical floating gate memory cells and select gates for a NOR architecture floating gate memory array in accordance with embodiments of the present invention. Figure 4A details a side view of a simplified vertical NOR architecture memory cell structure 404, a side view of a vertical NOR memory array 400 is detailed in Figure 4B. Figure 4C details an equivalent circuit schematic 420 of the vertical NOR architecture floating gate memory array 400, showing floating gate memory cells 402 and substrate connection 422. It is noted that the NOR architecture floating gate memory array 400 can be utilized in both EEPROM or Flash memories arrays and devices. As can be seen from Figures 4A and 4B, in a single vertical NOR architecture memory cell structure 404, two vertically formed transistors occupy the area that a single planar floating gate transistor would occupy (an area of 4F squared when viewed from above, each transistor having an area of 2F squared). Where “F” is the minimum resolvable photolithographic dimension in the particular process technology.

**[0044]** In Figure 4A, a vertically formed floating gate memory cell 402 and select gate 410 are coupled together in series in a vertical NOR architecture memory cell structure 404. In creating the vertical NOR architecture memory cell structure 404 a trench 430 is formed in a substrate 408. The vertical floating gate memory cell 402 and select gate 410 are then formed on the sidewalls of the trench 430. The vertical floating

gate memory cell 402 has a gate-insulator stack made of a tunnel insulator 420 formed on the surface of the sidewall, a floating gate 422 (typically of polysilicon) formed on the tunnel insulator 420, an intergate/interpoly insulator 424 formed over the floating gate 422, and a control gate 406 (typically formed in a control gate line, also known as a word line) formed over the intergate/interpoly insulator 424. In one embodiment, the substrate trench 430 is formed by patterning a masking material that is layered over the substrate 408 and anisotropically etching the trenches 430. The gate-insulator stack of the floating gate memory cell 402 is formed in one embodiment by successive layering of each of the materials of the gate insulator stack over the trench 430, followed by a mask and directional etch of the deposit of each layer to leave only the material deposited on the sidewall of the trench 430. In another embodiment, differing layers of the gate-insulator stack are formed and then masked and directionally etched in a single step.

**[0045]** The vertical select gate 410 has a gate-insulator stack made of an insulator 442 formed on the opposite sidewall of the trench 430 with a control gate 444 formed over the insulator 442. The gate-insulator stack of the select gate 410 is formed by successive layering of each of the materials of the gate insulator stack over the trench 430, as with the vertical floating gate memory cell 402, but skips the depositing of the tunnel insulator 420 and floating gate 422 layers. In one embodiment of the present invention the tunnel insulator 420 and the floating gate 422 of the floating gate memory cell 402 are formed and then the intergate/interpoly insulator 424/control gate 406 of the floating gate memory cell 402 and the insulator 442/control gate 444 of the select gate 410 are formed consecutively.

**[0046]** N+ doped regions 426 are formed at the raised areas at the top and at the bottom of the trenches 430 to form the source and drain regions for the vertical floating gate memory cell/gate-insulator stack 402 and select gate 410. The N+ regions also couple the memory cell 402 and select gate 410 together to form the vertical NOR memory structure 404 and additionally couple the vertical NOR architecture memory cell structure 404 to the bit line 412 and source line 414. It is noted that the N+

source/drain regions 426 may be formed before or after the formation of the floating gate memory cell 402 and select gate 410 gate-insulator stacks.

**[0047]** In Figure 4B, a vertical NOR architecture floating gate memory array 400 is formed from a series of vertical NOR architecture memory cell structures 404. Each vertical NOR architecture memory cell structures 404 having a vertically formed floating gate memory cell 402 and a coupled select gate 410, wherein the drain of the select gate is coupled to a bit line 412 and the source of the floating gate 402 is coupled to a source line 414.

**[0048]** In creating the vertical NOR architecture floating gate memory array 400 a series of substrate pillars 428 are formed in a substrate 408 with trenches 430 located between them. The vertical floating gate memory cells 402 and select gates 410 are then formed on the sidewalls of the pillars 428 within the trenches 430 to form the vertical NOR architecture memory cell structures 404. The vertical floating gate memory cells 402 and select gates 410 are formed in an alternating pattern (floating gate-select gate, select gate-floating gate, floating gate-select gate, etc.) such that each pillar 428 has either select gates 410 or floating gates formed on its sidewalls.

**[0049]** N+ doped regions 426 are formed at the top of the pillars 428 and at the bottom of the trenches 430 to form the source and drain regions. The N+ regions at the bottom of the trenches 430 couple the memory cell 402 and select gate 410 of each vertical NOR architecture memory cell structure 404 together. The N+ regions at the tops of the pillars 428 couple the drain of the select gate 410 and the source of the floating gate memory cell 402 of each vertical NOR architecture memory cell structure 404 to the bit lines 412 and source lines 414 respectively, so that the N+ regions on the top of the pillars 428 are coupled to either a source line 414 or a bit line 412. It is again noted that the N+ source/drain regions 426 may be formed before or after the formation of the floating gate memory cell 402 and select gate 410 gate-insulator stacks.

**[0050]** It is also noted that isolation regions, typically formed of an oxide insulator, can be used between adjacent rows of vertical NOR architecture memory cell structures 404 to isolate each row from its neighbors. These isolation regions can be extended into the substrate 408 to allow the formation of P-wells, where each P-well contains a

single row of vertical NOR architecture memory cell structures 404 that can be biased in isolation from the other rows of the array 400. It is also noted that the control gate/word address lines 406 and select lines 440 can cross these isolation regions so that each control gate/word address line 406 and select line 440 controls the operation of multiple floating gate memory cells 402 and select gates 410, respectively, across multiple rows of vertical NOR architecture memory cell structures 404.

**[0051]** As stated above, Figure 4C details an equivalent circuit schematic 420 of the vertical NOR architecture floating gate memory array 400, showing floating gate memory cells 402 and substrate connection 422. The vertical floating gate memory cells 402 and select gates 410 are formed in an alternating pattern (floating gate-select gate, select gate-floating gate, floating gate-select gate, etc.) so that the drain of the select gate 410 and the source of the floating gate memory cell 402 of each vertical NOR architecture memory cell structure 404 is coupled to a bit line 412 or a source line 414 respectively.

**[0052]** In the vertical NOR architecture floating gate memory array 400 of Figures 4A-4C, the channel length of each floating gate memory cell 402 and select gate 410 in a vertical NOR architecture memory cell structure 404 is determined by the depth of the trenches 430 and not by the minimum feature size. Due to the vertical form of the vertical NOR architecture floating gate memory array 400 and vertical NOR architecture memory cell structures 404 of embodiments of the present invention, a NOR architecture floating gate memory array can be produced that contain a vertical floating gate memory cell 402 and a coupled select gate 410 in the space that would be utilized by a single conventional planar floating gate memory cell.

**[0053]** The addition of a select gate 410 coupled between the bit line 412 and the drain of each floating gate memory cell 402 allows for the floating gate memory cell 402 to be isolated from the bit line 412 and thus has advantages in both programming and erasing the floating gate memory cells 402 of the vertical NOR architecture floating gate memory array 400. In erasing, the coupled select gate 410 allows for avoidance of overerasure issues with floating gate memory cells 402 by isolating each memory cell 402 behind a select gate 410 so that, even if a floating gate memory cell 402 is

overerased into depletion mode, it will not corrupt the reading of other memory cells 402 on its bit line 412 by flowing current. As the possibility of corruption of data reads due to overerasure is mitigated, this allows for the NOR architecture floating gate memory array 400 to speed up its erasure processes by using larger erase pulses (in time or voltage) or even utilizing only a single erase pulse. In addition, by allowing the increase of erasure pulse time and voltage, the number of erasure verifications required are reduced or even eliminated. The coupled select gate 410 also allows for the isolated erasure of one or more floating gate memory cells 402 allowing erasure of individual floating gate memory cells 402, one or more selected data words, data segments, or erase blocks.

**[0054]** In programming, the coupled select gate 410 allows for mitigation of programming disturb of floating gate memory cells 402 in the array 400 by the select gate 410 isolating the memory cells 402 from the bit line 412. This allows for longer and higher voltage programming pulses to be used without increasing the possibility of disturb issues.

**[0055]** Figures 5A-5D detail vertical floating gate cells, vertical select gates, and NAND architecture floating gate memory strings in accordance with embodiments of the present invention. Figure 5A details a side view of a simplified vertical NAND architecture floating gate memory string 504 with vertical select gates 510. Figure 5B details an equivalent circuit schematic 520 of the vertical NAND architecture floating gate memory string 504, showing floating gate memory cells 502 and substrate connection 534. Figure 5C details a side view of a simplified vertical NAND architecture floating gate memory array 500 and Figure 5D details an equivalent circuit schematic of one embodiment of the present invention. Again, as can be seen from Figures 5A and 5C, in a vertical NAND architecture memory string 504, two vertically formed transistors occupy the area that each planar transistor would occupy (an area of 4F squared when viewed from above, each transistor having an area of 2F squared). Where “F” is the minimum resolvable photolithographic dimension in the particular process technology. Since each transistor can store a single bit of data the data storage

density is one bit for each  $2F^2$  squared unit area. Thus, for example, if  $F=0.1$  micron then the storage density is 0.5 Giga bit per square centimeter.

**[0056]** In Figure 5A, a series of vertically formed floating gate memory cells 502 are coupled together in a series floating gate NAND string 504 (typically of 8, 16, 32, or more cells). In the vertical NAND floating gate memory array string 504 of Figures 5A-5D, a series of substrate pillars 528 are formed in a substrate 508 with trenches 530 located between them. The vertical floating gate memory cells 502 are then formed on the sidewalls of the pillars 528 within the trenches 530. Each vertical floating gate memory cell 502 is formed on the sidewalls of the substrate pillars 528 (for two floating gate memory cells 502 per trench 530) and has a gate-insulator stack made of a tunnel insulator 520 formed on the surface of the sidewall, a floating gate 522 (typically of polysilicon) formed on the tunnel insulator 520, an intergate/interpoly insulator 524 formed over the floating gate 522, and a control gate 506 (typically formed in a control gate line, also known as a word line) formed over the intergate/interpoly insulator 524.

**[0057]** In one embodiment the substrate pillars 528 and trenches 530 are formed by patterning a masking material that is layered over the substrate 508 and anisotropically etching the trenches 530. The gate-insulator stack of each floating gate memory cell 502 are formed in one embodiment by successive layering of each of the materials of the gate insulator stack over the pillars 528 and trenches 530, followed by a mask and directional etch of the deposit of each layer to leave only the material deposited on the sidewall of the pillars 528. In another embodiment, differing layers of the gate-insulator stack are formed and then masked and directionally etched in a single step.

**[0058]** N+ doped regions 526 are formed at the top of the substrate pillars 528 and at the bottom of the trenches 530 between each vertical floating gate memory cell/gate-insulator stack 502 to form the source and drain regions of the adjacent floating gate memory cells 502 and couple the memory cells 502 together to form the vertical NAND architecture memory string 504. It is noted that the N+ source/drain regions 526 may be formed before or after the formation of the floating gate memory cells/gate-insulator stack 502.

**[0059]** Select gates 510, that are coupled to gate select lines, are formed at either end of the NAND floating gate memory string 504 and selectively couple opposite ends of the NAND floating gate memory string 504 to a bit line contact 512 and a source line contact 514. The vertical select gates 510 have a gate-insulator stack made of an insulator 542 formed on a sidewall with a control gate 544 formed over the insulator 542. The gate-insulator stack of the select gates 510 are formed by successive layering of each of the materials of the gate insulator stack over the pillars 528 and trenches 530, as with the vertical floating gate memory cell 502, but skips the depositing of the tunnel insulator 520 and floating gate 522 layers. The N+ regions 526 also couple the first and last memory cell 502 of the vertical NAND architecture floating gate string 504 to the select gates 510 and additionally couple the vertical NAND architecture floating gate string 504 to the bit line 512 and source line 514.

**[0060]** As stated above, Figure 5B details an equivalent circuit schematic of the vertical NAND architecture floating gate memory array 500, showing the vertical floating gate memory cells 502, select gates 510, bit line 512 and source line 514 connections, and substrate connection 534, in accordance with embodiments of the present invention. As can be seen, the schematic provides the same equivalent circuit as that of a conventional planar NAND architecture floating gate memory string.

**[0061]** In Figure 5C, a section of vertical NAND architecture floating gate memory array 500 of one embodiment of the present invention is formed from a series of vertical NAND architecture floating gate memory cell strings 504. In Figure 5C, each pair of adjacent vertical NAND architecture floating gate memory cell strings 504 in the vertical NAND architecture floating gate memory array 500 are coupled through vertical select gates 510 to a common bit line 512 by a N+ doped region 526 formed at the top of a pillar 528.

**[0062]** It is also noted that isolation regions, typically formed of an oxide insulator, can be used between vertical NAND architecture floating gate memory cell strings 504 to isolate each string 504 from its neighbors. These isolation regions can be extended into the substrate 508 to allow the formation of P-wells, where each P-well contains a single vertical NAND architecture floating gate memory cell string 504 that can be

biased in isolation from the other strings or rows of the array 500. It is also noted that the control gate/word address lines 506 and select lines 540 can cross these isolation regions so that each control gate/word address line 506 and select line 540 controls the operation of floating gate memory cells 502 and select gates 510 respectively across multiple rows of vertical NAND architecture floating gate memory cell strings 504.

**[0063]** As stated above, Figure 5D details an equivalent circuit schematic of the vertical NAND architecture floating gate memory array of Figure 5C, showing floating gate memory cells 502 and adjacent sting 504 connection.

**[0064]** In the vertical NAND architecture floating gate memory array 500 of Figures 5A-5D, the channel length of each floating gate memory cell 502 and select gate 510 in a vertical NAND architecture memory string 504 is determined by the depth of the pillars 528 and trenches 530 and not by the minimum feature size. Due to the vertical form of the NAND architecture floating gate memory array 500 and NAND architecture memory strings 504 of embodiments of the present invention, a vertical NAND architecture floating gate memory array string 504 and select gates 510 can be produced that typically has twice the density for a given string horizontal run length than a corresponding planar NAND architecture floating gate memory array string.

**[0065]** The addition of a select gates 510 coupled between the bit line 512, source line 514, and the floating gate memory cells 502 of the vertical NAND architecture memory string 504 allows for the floating gate memory cells 502 of the vertical NAND architecture memory string 504 to be isolated from the bit line 512 and/or source line 514 and thus has advantages in both programming and erasing the vertical NAND architecture memory string 504. In erasing, the coupled select gates 510 allows for avoidance of overerasure issues with floating gate memory cells 502 by isolating each vertical NAND architecture memory string 504 behind one or more select gates 510 so that even if the floating gate memory cells 502 of the vertical NAND architecture memory string 504 are overerased into depletion mode operation they will not corrupt the reading of other memory cells 502 on other vertical NAND architecture memory strings 504 that are coupled to its bit line 512. As the possibility of corruption of data reads due to overerasure is mitigated, this allows for the vertical NAND architecture

floating gate memory array 500 to speed up erasure processes by using larger erase pulses or even a single erase pulse and by reducing or eliminating erasure verification. The coupled select gates 510 also allow for the isolated erasure of one or more floating gate memory cells 502 allowing erasure of individual floating gate memory cells 502, individual vertical NAND architecture memory strings 504, one or more selected data words, or erase blocks. In programming, the coupled select gates 510 allow for mitigation of programming disturb of floating gate memory cells 502 in the array 500 by the select gates 510 isolating the memory cells 502 of the vertical NAND architecture memory strings 504 from the bit line 512 and the source line 514. This allows for longer and higher voltage programming pulses to be used without an increased issue with of disturb problems.

**[0066]** Figures 6A-6C detail three dimensional views of vertical floating gate cells 602 and vertical select gates 610 of a vertical NAND floating gate memory array 600 in accordance with embodiments of the present invention at several mid-fabrication stages. It is noted that a formation process that is similar to the NAND process may be utilized for formation of a vertical NOR floating gate memory array 400 with the exception of placement and number of the select gates 610 and bit line and source line contacts. As stated above, in creating the vertical NAND floating gate memory array 600, a series of substrate pillars 628 are formed in a substrate 608 with trenches 630 located between them. The vertical floating gate memory cells 602 and select gates 610 are then formed on the sidewalls of the pillars 628 within the trenches 630. Between successive rows of substrate pillars 628, isolation regions 632 have been formed on the faces of the pillars 628 that are not utilized to form floating gate memory cells 602 or select gates 610 to isolate each row of vertical NAND floating gate memory strings 604 from the neighboring rows. These isolation regions 632 are typically formed of an oxide insulator.

**[0067]** As stated above, in creating each floating gate memory cell gate-insulator stack 602, a tunnel insulator 620 is formed on the surface of the sidewall, a floating gate 622 is formed on the tunnel insulator 620, an intergate/interpoly insulator 624 is formed over the floating gate 622, and a control gate 606 is formed over the intergate/interpoly

insulator 624. In creating each select gate gate-insulator stack 610, an insulator 642 is formed on the surface of the sidewall, and a control gate 644 is formed over the insulator 642.

**[0068]** In Figure 6A, the trenches 630 have been already formed by masking and anisotropically/directionally etching the trenches 630 in the substrate 608. N+ doped regions 626 have been formed at the top of the unformed substrate pillars 628 and at the bottom of the trenches 630 to form the source/drain regions of the floating gate memory cells 602. The gate-insulator stack of each floating gate memory cell 602 have been partially formed on the sidewalls of the trenches 630. In each trench 630, with the exception of the pillar 628 on which the select gates 610 are to be formed, are formed the tunnel insulator 620, the floating gate 622, and the intergate/interpoly insulator 624, by successive depositing, masking, and directional etching of layers of material.

**[0069]** In Figure 6B, the pillars 628 are formed and the space between each pillar in successive rows of NAND architecture floating gate memory strings 604 are filled with an oxide to form isolation regions 632. In forming the pillars 628, the rows of NAND architecture floating gate memory strings 604 are masked and directionally etched. This masking and etching process also divides the floating gate layer into individual floating gates 622.

**[0070]** In Figure 6C, the control gates/word lines 606 and select gates 610/select lines 640 are formed. In forming the control gates/word lines 606 and select gates 610/select lines 640, successive layers of insulator and polysilicon which will form the control gates/word lines 606 and select gates 610/select lines 640 is deposited over the pillars 628, trenches 630, and partially formed gate-insulator stacks of the floating gate memory cells 602 of the memory array 600. A layer of masking material is then formed over the polysilicon layer and patterned. The excess masking material is removed and the memory array 600 is anisotropically/directionally etched to remove the undesired portions of the deposited polysilicon and form the control gates/word lines 606 and select gates 610/select lines 640 on the sidewalls of the pillars 628 and trenches 630.

**[0071]** It is noted that the isolation regions 632 between the vertical NAND architecture floating gate strings 604 can be extended into the substrate 608 to allow the

formation of P-wells, where each P-well contains a single NAND string 604 and can be biased in isolation from the other strings 604 of the array 600. It is also noted that the control gates/word lines 606 and select gates 610/select lines 640 cross these isolation regions 632 so that each control gate/word address line 606 controls the operation of floating gate memory cells 602 and each select line 640 the operation of select gates 610 across multiple NAND memory strings 604.

**[0072]** In Figures 6A-6C, the substrate 608 of the vertical NAND architecture floating gate memory array 600 is P-doped. A substrate connection can be utilized that can allow for biasing of the P-doped substrate 608. It is noted that other forms of substrate doping, substrate biasing, and substrate types and regions (including, but not limited to silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor) in embodiments of the present invention are possible and should be apparent to those skilled in the art with the benefit of the present invention.

**[0073]** As noted above the programming of the floating gate memory cells of the vertical NAND and NOR architecture memory structures, strings, and arrays of embodiments of the present invention can be accomplished by conventional tunnel injection of electrons with a positive gate voltage with respect to the substrate or P-well. In another embodiment of the present invention, programming is accomplished by channel hot electron injection (HEI). Erasure of the floating gate memory cells of embodiments of the present invention can be accomplished by conventional tunneling or negative voltages applied to the control gate voltages with respect to the substrate or P-well. In alternative embodiments of the present invention, substrate enhanced hot electron injection (SEHE) can be utilized for floating gate memory cell programming and/or substrate enhanced band to band tunneling induced hot hole injection (SEBBHH) for floating gate memory cell erasure.

**[0074]** Figure 7 illustrates a functional block diagram of a memory device 700 that can incorporate the vertical NAND architecture floating gate memory array 500 or vertical NOR architecture floating gate memory cell array 400 of the present invention.

The memory device 700 is coupled to a processor 710. The processor 710 may be a microprocessor or some other type of controlling circuitry. The memory device 700 and the processor 710 form part of an electronic system 720. The memory device 700 has been simplified to focus on features of the memory that are helpful in understanding the present invention.

**[0075]** The memory device includes an array of vertical floating gate memory cells and select gates 730. In one embodiment, the memory cells are vertical floating gate memory cells and the memory array 730 are arranged in banks of rows and columns. The control gates of each row of memory cells is coupled with a wordline while the drain and source connections of the memory cells are coupled to bitlines. As is well known in the art, the connection of the cells to the bitlines depends on whether the array is a NAND architecture or a NOR architecture.

**[0076]** An address buffer circuit 740 is provided to latch address signals provided on address/data bus 762. Address signals are received and decoded by a row decoder 744 and a column decoder 746 to access the memory array 730. It will be appreciated by those skilled in the art, with the benefit of the present description, that the size of address input on the address/data bus 762 depends on the density and architecture of the memory array 730. That is, the size of the input address increases with both increased memory cell counts and increased bank and block counts. It is noted that other address input manners, such as through a separate address bus, are also known and will be understood by those skilled in the art with the benefit of the present description.

**[0077]** The memory device 700 reads data in the memory array 730 by sensing voltage or current changes in the memory array columns using sense/buffer circuitry 750. The sense/buffer circuitry, in one embodiment, is coupled to read and latch a row of data from the memory array 730. Data input and output buffer circuitry 760 is included for bi-directional data communication over a plurality of data connections in the address/data bus 762 with the processor/controller 710. Write circuitry 755 is provided to write data to the memory array.

**[0078]** Control circuitry 770 decodes signals provided on control connections 772 from the processor 710. These signals are used to control the operations on the memory

array 730, including data read, data write, and erase operations. The control circuitry 770 may be a state machine, a sequencer, or some other type of controller.

**[0079]** Since the vertical floating gate memory cells of the present invention use a CMOS compatible process, the memory device 700 of Figure 7 may be an embedded device with a CMOS processor.

**[0080]** The memory device illustrated in Figure 7 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of internal circuitry and functions of memories are known to those skilled in the art.

**[0081]** It is also noted that other vertical NAND and NOR architecture floating gate memory strings, arrays, and memory devices in accordance with embodiments of the present invention are possible and should be apparent to those skilled in the art with benefit of the present disclosure.

#### Conclusion

**[0082]** EEPROM memory devices and arrays have been described that facilitate the use of vertical floating gate memory cells and select gates in NOR or NAND high density memory architectures. Memory embodiments of the present invention utilize vertical select gates and floating gate memory cells to form NOR and NAND architecture memory cell strings, segments, and arrays. These memory cell architectures allow for an improved high density memory devices or arrays with integral select gates that can take advantage of the feature sizes semiconductor fabrication processes are generally capable of and allow for appropriate device sizing for operational considerations. The memory cell architectures also allow for mitigation of disturb and overerasure issues by placing the floating gate memory cells behind select gates that isolate the memory cells from their associated bit lines and/or source lines.

**[0083]** Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement, which is calculated to achieve the same purpose, may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the

present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.